Jagadish D. N.

Curriculum Vitae

✉ *jagadishdn@iiitdwd.ac.in*
Asst. Professor @ IIIT Dharwad, age - 41

A striving soul to revere knowlegde and its essence to human race,
by embracing, contributing and taking knowledge to masses.

Education

2011–2017 **Doctor of Philosophy**, *Electronics & Communication Engineering*, National Institute of Technology Karnataka.
Thesis title– Design of low power successive approximation register ADC

2005–2007 **Master of Technology**, *Electronics & Communication Engg.*, Visveswaraya Technological University, Karnataka, *First Class Distinction*.
Specialized in VLSI Design and Embedded Systems

1995–1999 **Bachelor of Engineering**, *Electrical & Electronics Engg.*, Bangalore University, karnataka, *First Class*.

Experience

2016–Present **Faculty**, Indian Institute of Information Technology, Dharwad.
Serving as an Assistant Professor and HoD of department of E&C Engg. since August 2016. Apart from creating interest amongst the undergraduate students in field of electronics by delivering lectures, have been actively involved in setting up various electronic laboratories. Have taken up several administrative responsibilities, such as, Controller of Examination and Cultural & Sports Committee Chairman. Have been member of various committes, such as, Purchase, Curriculum, Library and Website; with a vision to support overall development of the Institute students.

2011–2016 **Research Scholar**, National institute of Technology karnataka, Surathkal.
Did research in analog and mixed signal circuit domain. Have introduced two novel architectures to realize area and energy efficient analogue-to-digital converter. One of the design is analog circuit intensive, uses switched capacitor circuit; the other is digital circuit intensive. The designs are implemented in CMOS 90nm technology. A second order noise-shaping SAR converter architecture using switched capacitor circuit is proposed as well.

2007–2011 **Faculty**, BMS Institute of Technology, Bangalore.
Served the E&E Engg. department in capacities of Lecturer (3-yr) and later as assistant professor under 5^{th} pay commission (1-yr). Had been able to inspire students to excel in the field of electronic circuits, control theory, signal processing and much more.

Research Interests

Analog & Mixed Signal VLSI, Neuromorphic Computing and Machine Learning.

Patents filed

1 "Successive Approximation Register Analog To Digital Converter Circuit And Conversion Method Thereof", Indian patent application 4777/CHE/2013, examination awaited.

2 "Switched Capacitor Integrator Based Successive Approximation Register Analog To Digital Converter Circuit And Conversion Method Thereof", Indian patent application 3549/CHE/2014, examination awaited.

Publications

International Journals

1 Jagadish, D. N., Laxminidhi, T., and M. S. Bhat (2018). 11.39 fJ/conversion-step 780 kS/s 8 bit Switched Capacitor based Area and Energy Efficient SAR ADC in 90 nm complementary metal oxide semiconductor. IET Circuits, Devices and Systems, **12**(3), 249–255.

2 Jagadish, D. N., and M. S. Bhat (2018). 14.5 fJ/conversion-step 9-bit 100-kS/s non-binary weighted dual capacitor array based area and energy efficient SAR ADC in 90 nm CMOS. IET Circuits, Devices and Systems, **12**(6), 671–680.

3 Jagadish, D. N., and M. S. Bhat (2015). Low energy and area efficient nonbinary capacitor crray based successive approximation register analog-to-digital converter. *Journal of Low Power Electronics*, **11**(3), 436–443.

International Conference papers

1 Jagadish, D. N. and M. S. Bhat, "Low energy and area efficient nonbinary capacitor array based SAR ADC," in Proc. 5th International Symposium on Electronic System Design (ISED), December 2014, pp. 54–57.

2 Jagadish, D. N. and M. S. Bhat, "A low voltage inverter based differential amplifier for low power switched capacitor applications," in Proc. 5th International Symposium on Electronic System Design (ISED), December 2014, pp. 58–62.

3 Sridhar, R. N., Jagadish, D. N. and M. S. Bhat, "A low-energy area-efficient dual channel SAR ADC using common capacitor array technique," in Proc. IEEE Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER), August 2016, pp. 148–152.

Research Proposal

1 Submitted a proposal as PI to Science and Engineering Research Board, GoI, Smart Irrigation planning and management using geophysical and meteorological data, CRG/2018/003436/EEC with Dr. Arun Chauhan and Dr. Lakshman Mahto as Co-PIs.

2 Submitted a proposal for centre of Excellence to Ministry of Home Affairs, GoI, Detection and prediction of cyber crime against women and childern, with Dr. Arun Chauhan as PI and Dr. Kavi Mahesh and Dr. Lakshman Mahto as other Co-PIs, April 2018.

3 Submitted a proposal for establishing Neural Information Processing and Robotics laboratory under VGST grant, K-FIST-L2, Oct 2018.

Administration

1 Invitee, Institute Senate (since 2nd December 2017)

2 Head, Dept. of Electronics & Communication Engg. (23/08/2016 to present, 5- Semesters)

3 Controller of Examination (26/09/2016 to present, 5- Semesters)

4 Chairman, Cultural & Sports Committee (22/02/2017 to present, 4- Semester)

5 Member, Purchase Committee (2016 to 28/01/2019, 5- Semester)

6 Member, Curriculum Committee (06/02/2017 to present, 4- Semesters)

7 Member, Library Committee (16/08/2016 to present, 5- Semesters)

8 Member, Selection Committee, selection of non-teaching staff of the Institute (03/11/2016 & 11/03/2017)and screening committee, faculty recruitment 2018.

9 Member, Disciplinary Committee

10 Member, Technical Committee (for purchase)

11 Assisted in framing/ verifying Institute Academic regulations, Statutes, MoU with MHRD, Academic calendar, organizing workshops, seminars, industrial visit, students orientation program and other such events and part of student admission team for the year 2018-19.

12 Coordinator, Ek Bharat Shresta Bharat and Paryatan parv programs of Govt. of India

Academic engagement @ IIIT Dharwad

The details are in the sheet attached.

Personal/Additional information

Scholarship	Awardee of MHRD fellowship to carry out research. Have delivered lectures and handled laboratory sessions at NITK.
Public service	Served Election Commission of India by training manpower and conducting 2009 loksabha election.
Parents name	Smt. Kempamma and Shri. Narasimaiah.
Nationality	Indian
Religion	Hindu
Category	IIIA
Caste	Vokkaliga
Date of Birth	29/08/1977
Languages	Fluent in english, hindi and kannada.
Hobbies	Attending talks, mentoring, involving in sports activities ...
Family	Blessed to live with caring parents, spouse and two kids.
References	Dr. M. S. Bhat, Professor, Dept. of E&C Engg., National Institute of Technology karnataka, Surathkal. Email: msbhat_99@yahoo.com, Phone 9448887426.
	Dr. Muralidhara Kulkarni, Professor, Dept. of E&C Engg., National Institute of Technology karnataka, Surathkal. Email: mkuldce@gmail.com, Phone 9686588668.
	Dr. Vijay Bhaskar Semwal, Assistant professor, Dept. of CSE, National Institute of Technology, Bhopal. Email: vsemwal@gmail.com, Phone 7541805885.

Date : 04 Feb 2019

Details of academic engagement

- Odd Semester (August-2016 to December-2016) Total Credits- **8.5** Credits

S.No.	Name Of Subject	Branch and Semester	No of students	Credit
1	Analog Electronics I	ECE- 3rd	15	3
2	Basic Circuit Theory	CSE+ECE- 1st	25	4
3	Analog Electronics I lab & Incharge	ECE- 3rd	15	1.5

- Even Semester (January-2017 to June-2017) Total Credits- **7.5** Credits

S. No.	Name Of Subject	Branch and Semester	No of students	Credit
1	Analog & Digital Comm.	ECE - 4th	15	3
2	Analog & Digital Comm. Lab & Incharge	ECE - 4th	15	1.5
3	Control Systems lab & Incharge	ECE - 4th	15	1.5
4	Analog Electronics II lab	ECE - 4th	15	1.5

- Odd Semester (August-2017 to December-2017) Total Credits- **09** Credits

S. No.	Name Of Subject	Branch and Semester	No of students	Credit
1	Analog Electronics I	ECE- 3rd	11	3
2	Introduction to VLSI Design	ECE - 5th	15	3
3	Analog Electronics I lab & Incharge	ECE- 3rd	11	1.5
4	Introduction to VLSI Design lab & Incharge	ECE - 5th	15	1.5

- Even Semester (January-2018 to February-2018) Total Credits- **7.5** Credits

S. No.	Name Of Subject	Branch and Semester	No of students	Credit
1	Control Systems	ECE - 4th	10	3
2	Computer Architecture	CSE+ECE - 2nd (shared)	63	1.5
3	Control Systems lab & Incharge	ECE - 4th	10	1.5
4	Computer Architecture lab & Incharge	CSE+ECE - 2nd	63	1.5
5	Supervisor of mini projects – 02 groups	CSE & ECE - 6th	04	4

- Odd Semester (August-2018 to December-2018) Total Credits- **8.5** Credits

S. No.	Name Of Subject	Branch and Semester	No of students	Credit
1	Analog Electronics I	ECE- 3rd	28	3
2	Introduction to VLSI Design	ECE - 5th	10	3
3	Analog Electronics I lab & Incharge	ECE- 3rd	28	1
4	Introduction to VLSI Design lab & Incharge	ECE - 5th	10	1.5
5	Supervisor of mini projects – 02 groups	CSE & ECE - 7th	04	4

- Even Semester (Jan-2019 to May-2019) Total Credits- **04** Credits

S. No.	Name Of Subject	Branch and Semester	No of students	Credit
1	Computer Architecture	CSE- 1st	83	3
2	Computer Architecture Lab & Incharge	CSE- 1st	83	1
3	Supervisor of major projects – 02 groups	CSE & ECE - 8th	06	16

Additionally I have offered 02 summer courses, internships to 02 PG students from KLE Technical University.